



IFW

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of)
Edwin C. Kan et al.) Group Art Unit No. 2818
Application No. : 10/718,662) Examiner:
Filed : November 24, 2003)
For : Multibit Metal)
Nanocrystal Memories)
and Fabrication)

INFORMATION DISCLOSURE STATEMENT

Honorable Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

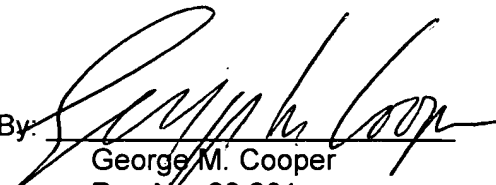
Pursuant to the provisions of 37 CFR 1.97 and 1.98, applicants hereby submit the documents listed on the attached PTO-1449A and PTO-1449B.

Copies of the listed publications are enclosed; copies of U.S. patents have not been included but will be furnished upon request.

Respectfully submitted,

Edwin C. Kan et al.
Applicant

JONES, TULLAR & COOPER, P.C.
Attorneys for Applicant

By: 
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July 21, 2004
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Substitute for form 1449A/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

Sheet	1	of	1
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Complete if Known

Application Number	10/718,662
Filing Date	November 24, 2003
First Named Inventor	Edwin C. Kan
Group Art Unit	2818
Examiner Name	
Attorney Docket Number	CRF D-2768/Kan

U.S. PATENT DOCUMENTS

[illegible]

FOREIGN PATENT DOCUMENTS

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Examiner
Signature

Date	
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*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

¹ Unique citation designation number. ² See attached Kinds of U.S. Patent Documents. ³ Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). ⁴ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁵ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. ⁶ Applicant is to place a check mark here if English language Translation is attached.

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**"INFORMATION DISCLOSURE
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Sheet

1

of

2

Complete if Known

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OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS

Examiner Initials ¹	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
	1	J.R. Tucker, "Schottky barrier MOSFETs for Silicon nanoelectronics," Advanced Workshop on Frontiers in Electronics, WOFE'97 Proceedings, pp. 97-100, 1997.	
	2	C. Wang, J.P. Snyder and J.R. Tucker, "Sub-40 nm PtSi Schottky source/drain metal-oxide-semiconductor field-effect transistors," Appl. Phys. Lett, vol. 74, pp1174-6, 1999.	
	3	V. Narayanan, Z. Liu, Y.M.N. Shen, M. Kim and E.C. Kan, "Reduction of metal-semiconductor contact resistance by embedded nanocrystals," IEDM Tech. Dig., pp. 87-90, 2000.	
	4	E.C. Kan and Z. Liu, "Directed self-assembly process for nano-electronic devices and interconnect," Superlattices and Microstructures, vol. 27, pp. 473-9, 2000.	
	5	Z. Liu, M. Kim, V. Narayanan, and E.C. Kan, "Process and device characteristics of self-assembled metal nano-crystal EEPROM," Superlattices and Microstructures, vol. 28, pp. 393-9, 2000.	
	6	Z. Suo and Z. Zhang, Epitaxial films stabilized by long range forces," Phys. Rev. B, vol. 58, pp. 5116-20, 1998.	
	7	D.A. Bonnell, Y. Liang, M. Wagner, D. Carroll and M. Buhle, "Effect of size dependent interface properties on stability of metal clusters on ceramic substrates," Acta Mater., vol. 46, pp. 2263-70, 1998.	
	8	Z. Liu, V. Narayanan, M. Kim, G. Pei and E.C. Kan, "Low programming voltages and long retention time in metal nanocrystal EEPROM devices," 59th DRC Tech. Dig., pp. 79-80, 2001.	
	9	H.C. Lin, E.C. Kan, T. Yamanaka & C.R. Helms, "Modeling and characterization of Si/SiO ₂ interface roughness," VLSI Tech. Symp., Kyoto, Japan, June 1997.	
	10	J. Kedzierski, P. Xuan, E.H. Anderson, J. Bokor, T.J. King and C. Hu, "Complementary silicide source/drain thin-body MOSFETs for the 20nm gate length regime," IEDM Tech. Dig., pp. 57-60, 2000. :	
	11	J. Kedzierski, P. Xuan, V. Subramanian, E.H. Anderson, J. Bokor, T.J. King and C. Hu, "A 20-nm gate-length ultra-thin body p-MOSFET with silicide source/drain," Si Nanoelectronics Workshop, VLSI Tech. Symp., pp. 13-15, Honolulu, Hawaii, June 2000	

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Signature

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1 Unique citation designation number. 2 Applicant is to place a check mark here if English language Washington Burden Hour Statement. This form is estimated to take 2.0 hours to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, Patent and Trademark Office, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Assistant Commissioner for Patents, Washington, DC 20231.